

Application No.: 10/830,107

REMARKS

Claim 1 is the sole independent claim and stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Sawada '591 ("Sawada") in view of Applicant's admitted prior art ("AAPA"). This rejection is respectfully traversed for the following reasons.

Claim 1 recites in pertinent part, "a digital equalizer for performing wave-form equalization to the first digital signal and outputting a second digital signal ... a clock extraction circuit for extracting a synchronous clock signal *from the second digital signal* and outputting the extracted clock signal to the A/D converter and the digital equalizer ... wherein the clock extraction circuit outputs to the A/D converter and the digital equalizer a sampling clock signal having an n times higher frequency than a frequency which defines a channel clock (where n is 2 or a larger integer than 2)" (emphasis added). The Examiner relies on the digital filter 538 of Sawada as the claimed "digital equalizer." However, as clearly shown in Figure 32 of Sawada, the alleged clock extraction circuit of Sawada does not extract a clock signal from the alleged second digital signal output from the alleged digital equalizer 538. That is, Figure 32 of Sawada does not illustrate that any signal extraction occurs from the *output* of the alleged "digital equalizer" 538. Indeed, it appears that digital filter 538 of Sawada operates at a same frequency as that of a channel clock as the clock frequency f_s/M for the filter 538 is the same as a frequency of the channel clock. In sum, Sawada does not disclose or suggest a structure in which a digital equalizer operates at a higher frequency than that of a channel clock.

According to one aspect of the present invention, it can be made possible to operate the digital equalizer at a higher frequency than that of the channel clock (*see, e.g.,* Fig. 1 of Applicants' drawings). With such a structure, the present invention can make it possible for wave-form equalization to the first digital signal obtained through the oversampling to be

Application No.: 10/830,107

performed with high accuracy according to the value n for an oversampling rate. As a result, a weak analog signal output from the optical pickup can be converted into a digital signal with high accuracy while a circuit scale is reduced (*see, e.g.*, page 13, line 24 - page 14, line 4 of Applicants' specification). Only Applicants have recognized and considered the aforementioned effect, and conceived of a structural configuration by which such an effect can be realized. The cited prior art is silent as to such an effect much less suggest the structural configuration needed to realize such an effect.

The Examiner is directed to MPEP § 2143.03 under the section entitled "All Claim Limitations Must Be Taught or Suggested", which sets forth the applicable standard for establishing obviousness under § 103:

To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. (citing *In re Royka*, 180 USPQ 580 (CCPA 1974)).

In the instant case, the pending rejection does not "establish *prima facie* obviousness of [the] claimed invention" as recited in claim 1 because the proposed combination fails the "all the claim limitations" standard required under § 103.

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.*, 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as claim 1 is patentable for the reasons set forth above, it is respectfully submitted that all claims dependent thereon are also patentable. In addition, it is respectfully submitted that the dependent claims are patentable based on their own merits by adding novel and non-obvious features to the combination.

Application No.: 10/830,107

Based on the foregoing, it is respectfully submitted that all pending claims are patentable over the cited prior art. Accordingly, it is respectfully requested that the rejections under 35 U.S.C. § 103 be withdrawn.

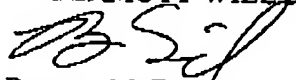
CONCLUSION

Having fully responded to all matters raised in the Office Action, Applicants submit that all claims are in condition for allowance, an indication for which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP



Ramyar M. Farid
Registration No. 46,692

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 RMF:MaM
Facsimile: 202.756.8087
Date: May 8, 2007

Please recognize our Customer No. 20277
as our correspondence address.